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CHAPTER 4 SOLUTIONS 9 effort should be about 4. This design has imbalanced delays and excessive efforts. The path effort is F = 12 * 6 * 9 = 648. The best number of stages is 4 or 5. One way to speed the circuit up is to add a buffer (two inverters) at the end. The gates should be resized to bear efforts of f = 648 1/5 = 3.65 each.

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~~Solved: The following exercise are specific to ...~~

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SOLUTIONS 14 searching.) Silver has better conductivity than copper and gold while having poorer conductivity than copper, has good immunity to oxidization. The reason for not using gold or silver is that they both have the property that they can migrate and enter the silicon. This alters CMOS device characteristics in undesirable ways.

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B1. Design simulated experiments using Cadence to verify

the integrity of a CMOS circuit and its layout. C1. Design digital circuits that are manufacturable in CMOS. K1. Apply the Cadence VLSI CAD tool suite layout digital circuits for CMOS fabrication and verify said circuits with layout paarasitic elements. K2, C2.

ESE570 Digital VLSI Circuits - Penn Engineering

Unformatted text preview: EL 5473 Introduction to VLSI Design Homework Assignment 2 Due beginning of Class February 9, 2010 1.(Problem 2.1 in text) Consider an nMOS transistor in a 0.6 ?m process with W/L= 4/2 ? (i.e., 1.2/0.6 ?m). In this process, the gate oxide thickness is 100 Å and the mobility of electrons is 350 cm2/Vs.

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The basics and applications of VLSI design from STA, PDA and VLSI Testing along with FPGA based prototyping are covered in a comprehensive manner. The latest technology used in VLSI design is discussed along with the available tools for FPGA prototyping as well as ASIC design. Each unit contains technical questions with solutions at the end.